What is claimed is:

1. Method for manufacturing a bipolar transistor having a polysilicon emitter, comprising:

generating a collector region of a first conductivity type and a basis region of a second conductivity type adjoining thereto in a semiconductor substrate;

applying a polycrystalline layer of a polycrystalline semiconductor material of the second conductivity type doped with doping atoms on the substrate, so that a portion of the basis region is exposed;

applying at least one insulating layer of an insulating material on the polycrystalline layer;

patterning the at least one insulating layer such that at least one section of the basis region is exposed;

generating a further polycrystalline layer of a polycrystalline semiconductor material of the first conductivity type heavily doped with doping atoms such that the exposed section is essentially covered, wherein the polycrystalline layer and the further polycrystalline layer are isolated by the insulating layer;

generating a highly conductive layer of a highly conductive material on the further polycrystalline layer to form an emitter double layer with the same;

effecting, via a temperature treatment, that at least part of the doping atoms of the second conductivity type of the

polycrystalline layer get into the semiconductor substrate to electrically connect the base region to the polycrystalline layer;

effecting that at least part of the doping atoms of the first conductivity type of the heavily doped further polycrystalline layer get into the basis region to generate an emitter region of the first conductivity type;

structuring the emitter double layer for generating an emitter terminal area;

contacting the emitter terminal area with an contact terminal, wherein the layer and the contact terminal vary, comprising the following substeps:

applying an insulating material on the emitter terminal area; and

etching a contact via into the insulating material, wherein the highly conductive layer in the emitter terminal area is effective as stop layer for the via etching.

2. Method in accordance with claim 1, wherein the step of effecting that at least part of the doping atoms of the first conductivity type of the heavily doped further polycristalline layer gets into the basis region, will be performed by means of tempering.

3. Method in accordance with claim 1, wherein the highly conductive layer consists of a material having comparative processing properties as the semiconductor material.

4. Method in accordance with claim 1, wherein the step of effecting that at least part of the doping atoms of the first conductivity type of the heavily doped further polycrystalline layer get into the basis region will be performed before or after the step of generating the highly conductive layer.